

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 **Claim 1 (Original):** A semiconductor device
2 comprising a substrate having an insulating layer formed on
3 a surface thereof, a semiconductor material layer located
4 on a surface of the insulating layer, a trench that extends
5 from a surface of the semiconductor material layer through
6 the insulating layer and into the substrate, an insulating
7 liner located on the side walls and the base of the trench,
8 and an in-fill of thermally-conductive material within the
9 insulating liner, wherein the insulating liner, the in-fill
10 material and the distance over which the trench extends
11 into the substrate are such as to promote flow of heat from
12 the semiconductor material layer to the substrate, the
13 insulating liner completely surrounding the in-fill
14 material at least where the trench extends into the
15 substrate, and said distance is at least 1 μm .

1 **Claim 2 (Original):** A semiconductor device is
2 claimed in claim 1, wherein said distance lies within the
3 range of from 1 μm to 5 μm .

1 **Claim 3 (Original):** A semiconductor device is
2 claimed in claim 2, wherein said distance lies within the
3 range of from 3 μm to 5 μm .

1 **Claim 4 (Original):** A semiconductor device as
2 claimed in any one of claims 1 to 3, wherein there are two
3 trenches, each of which has the features defined in
4 claim 1, and wherein an active device is formed in the
5 semiconductor material layer between the two trenches.

1 **Claim 5 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to ~~[[4]]~~ 3, wherein there
3 are a plurality of trenches, each of which has the features
4 defined in claim 1, and wherein a respective active device
5 is formed in the semiconductor material layer between each
6 pair of adjacent trenches.

1 **Claim 6 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to ~~[[5]]~~ 3, wherein the
3 semiconductor material layer is a silicon layer.

1 **Claim 7 (Original):** A semiconductor device as
2 claimed in claim 6, wherein the silicon layer is of single
3 crystal formation.

1 **Claim 8 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to [[7]] 3, wherein the
3 substrate is a silicon substrate.

1 **Claim 9 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to [[8]] 3, wherein the
3 insulating layer is a silicon oxide layer.

1 **Claim 10 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to [[9]] 3, wherein the
3 ~~or each~~ liner is constituted by an outer layer of silicon
4 oxide and an inner layer of silicon nitride.

1 **Claim 11 (Currently amended):** A semiconductor device
2 as claimed in claim 10, wherein the ~~or each~~ outer silicon
3 oxide layer has a thickness of substantially 1,000 [[A°]]
4 Å, and the ~~or each~~ inner silicon nitride layer has a
5 thickness of substantially 300 [[A°]] Å.

1 **Claim 12 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to [[11]] 3, wherein the
3 in-fill material is polysilicon.

1 **Claim 13 (Currently amended):** A semiconductor device
2 as claimed in claim 12, wherein the width of the ~~or each~~
3 trench is substantially 0.8 µm.

1 **Claim 14 (Currently amended):** A semiconductor device
2 as claimed in any one of claims 1 to 13, wherein the
3 thickness of the ~~or each~~ liner is at least an order of
4 magnitude less than the thickness of the insulating layer.